LISTING OF SPECIFICATION AMENDMENTS

Please replace paragraph [0008] with the following amended paragraph:

[0008] Domino logic gates are a popular dynamic logic family, in which an inverting static gate is inserted between successive dynamic gates. Standard domino logic inserts an inverter between the dynamic gates while compound domino logic inserts multiple input complementary gates. The dynamic/static gate pair is known as a domino gate, although it is in fact constructed from two gates. A series of connected domino gates precharge simultaneously as if setting up a set of dominos. During evaluation, the first dynamic gate falls causing the static gate to rise which then causes the next dynamic gate to fall and its static gate to rise, much like a chain of toppling dominos. It is common practice in domino logic design to divide a pipeline 2 of series-connected domino gates 4 into "cells" 6 each of which is controlled by a respective clock phase Φ, as may be seen in FIG. 1. Each cell 6 may contain one or more dynamic logic gates 8. As may also be seen in FIG. 1, cells 6a controlled by clock phase $\Phi 1$ may be referred to as "phase 1 logic"; cells 6b controlled by clock phase $\Phi 2$ may be referred to as "phase 2 logic", and cells 6c controlled by clock phase $\Phi 3$ may be referred to as "phase 3 logic".

Please replace the Heading between paragraphs [0079] and [0080] with the following amended Heading:

~~3.2.7~~ **Dynamic Cascaded Domino-Precharge/AND-Evaluate**